

HIGH PERFORMANCE STRESS-ENHANCED
MOSFETs USING Si:C and SiGe EPITAXIAL SOURCE/DRAIN
AND METHOD OF MANUFACTURE

ABSTRACT

A semiconductor device and method of manufacturing a semiconductor device. The semiconductor device includes channels for a pFET and an nFET. A SiGe layer is selectively grown in the source and drain regions of the pFET channel and a Si:C layer is selectively grown in source and drain regions of the nFET channel. The SiGe and Si:C layer match a lattice network of the underlying Si layer to create a stress component. In one implementation, this causes a compressive component in the pFET channel and a tensile component in the nFET channel.

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